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PATENT APPLICATION

ATTORNEY DOCKET NO. 10991989-1

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IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal Letter

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

JC564 U.S. PTO
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01/27/00

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): (X) Utility ( ) Design
(X) original patent application,
( ) continuation-in-part application

INVENTOR(S): **M. Jason Welch et al**

TITLE: **A Method Of Integrated Circuit Construction With Port Alignment And Timing Signal Buffering Within A Common Area**

Enclosed are:

(X) The Declaration and Power of Attorney. (X) signed ( ) unsigned or partially signed

(X) 4 sheets of drawings (one set) ( ) Associate Power of Attorney

( ) Form PTO-1449 ( ) Information Disclosure Statement and Form PTO-1449

( ) Priority document(s) ( )(Other) _____ (fee $_____)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	20 — 20	0	X $18	$ 0
INDEPENDENT CLAIMS	3 — 3	0	X $78	$ 0
ANY MULTIPLE DEPENDENT CLAIMS	0		$260	$ 0
		BASIC FEE: Design $310.00); Utility $690.00)		$ 690
			TOTAL FILING FEE	$ 690
			OTHER FEES	$
			TOTAL CHARGES TO DEPOSIT ACCOUNT	$ 690

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I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

By _____

Typed Name: **Kimberly D. Taylor**

Respectfully submitted,

M. Jason Welch et al

By _____

Cynthia S Mitchell

Attorney/Agent for Applicant(s)
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Date: Jan. 26, 2000

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Rev 12/99 (TransNew)

- Attach as First Page to Transmitted Papers -

A METHOD OF INTEGRATED CIRCUIT CONSTRUCTION WITH PORT ALIGNMENT AND TIMING SIGNAL BUFFERING WITHIN A COMMON AREA

TECHNICAL FIELD

The present invention is generally related to an integrated circuit having provisions for aligning ports developed using different layout methodologies and, more particularly, to an integrated system and method for aligning ports and providing for signal buffering within a common area of integrated circuit real estate.

BACKGROUND OF THE INVENTION

It is common in integrated circuit design for various methodologies to be utilized in laying out the signal wiring, or routing, which forms signal paths for signals to travel. Unfortunately, because of the inherent differences in these methodologies, it is common for there to be resulting mismatches in port alignments. As a result, the ports on various blocks of circuitry on an integrated circuit may not precisely line up for easy and direct interconnection. Thus, efforts must be taken to provide for an interface to link the different pieces of circuitry. This typically entails additional wiring to link the mis-aligned ports.

In order to combat the degradation in signal quality due to long signal paths, it is common to buffer the signals in order to retain proper signal timing and amplitude. Buffering of signals has typically been carried out separately from providing for linking

of mis-aligned ports. This has resulted in integrated circuit real estate being utilized separately for aligning mis-aligned ports and for providing for appropriate buffering. As integrated circuit real estate is typically at a premium, addressing these two issues separately has meant greater usage of integrated circuit real estate.

Fig. 1 illustrates an example of two sets of ports from separate blocks of circuitry on an integrated circuit 200. Here it can be seen that a first set of ports 10, 11, 12 and 13 are located in a one area 1 on the integrated circuit 200. A second set of ports 14, 15, 16 and 17 are provided in a separate area 2 of integrated circuit 200. It will be noted that ports 10 and 14 represent a signal path A; that ports 11 and 15 represent a signal path B; that ports 12 and 16 represent a signal path C and that ports 13 and 17 represent a signal path D. Axes 100, 101, 102 and 103 help to show that the above pairs of ports do not directly align with one another.

With reference to Fig. 2 one typical technique of aligning ports is shown. Here a linking area 25 is utilized wherein bridge traces 20, 21, 22 and 23 are used to connect a first set of ports (ports 10, 11, 12 and 13, respectively) with a second set of ports (ports 14, 15, 16 and 17 respectively), via wiring traces (30, 31, 32 and 33 respectively) and signal buffering blocks (40, 41 42 and 43 respectively) in common area 35. The use of linking area 25 to provide for bridging traces 20, 21, 22 and 23 separate from common area 35 requires consumption of integrated circuit real estate which could otherwise be devoted to other purposes. This is expensive and wasteful, particularly with complex integrated circuits in which thousands upon thousands of semiconductor gates are implemented on the integrated circuit.

Thus, a heretofore unaddressed need exists in the industry to address the aforementioned deficiencies and inadequacies.

SUMMARY OF THE INVENTION

The present invention provides an integrated system and method for aligning mis-aligned ports within an integrated circuit designed using various layout methodologies.

Briefly described, in architecture, the system can be implemented as follows. There is provided an output port for transmitting a signal to a second port. The second port is designed to receive the signal. There is provided an alignment link for electrically connecting the first port with the second port. The alignment link is made up of a signal buffer for buffering a signal traveling along the alignment link between the first port and the second port.

The present invention can also be viewed as providing a method for aligning ports in an integrated circuit. In this regard, the method can be broadly summarized by the following steps: extending a first port from one area into a common area; extending a second port from another area into the common area; linking the first port to the second port within the common area via an alignment link composed of a wiring trace and a signal buffer.

Other features and advantages of the present invention will become apparent to one with skill in the art upon examination of the following drawings and detailed description. It is intended that all such additional features and advantages be included herein within the scope of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present invention. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

FIG. 1 is a diagram illustrating mis-aligned ports.

FIG. 2 is a diagram illustrating a typical technique of aligning mis-aligned ports.

FIG. 3 is a diagram illustrating an integrated circuit in accordance with the present invention.

FIG. 4 is a diagram illustrating multiple-levels of integrated circuit real estate.

DETAILED DESCRIPTION

The present invention is directed to an integrated circuit wherein provisions for aligning ports developed using different layout methodologies share common areas of integrated circuit real estate with buffering circuitry used to buffer signals so as to prevent degradation of signal quality.

Fig. 3 illustrates an integrated circuit 200 in accordance with the present invention. As shown by Fig. 3, there is provided a common area 35, a first area 1 and a second area 2. Each of these areas represents separate non-overlapping areas of real estate on the integrated circuit. There are provided a set of output ports 10, 11, 12 and 13

in first area 1. These output ports represent outputs for one block of circuitry. A second set of ports 14, 15, 16 and 17 are provided in a second area 2. These ports represent input ports to a second block of circuitry on integrated circuit 200. It should be noted that output ports 10, 11, 12 and 13, as well as input ports 14, 15, 16 and 17 could be implemented as bi-directional bus connections. Output ports 10, 11, 12 and 13 are extended directly into common area 35. Common area 35 is a multilevel area of real estate in which signal buffering blocks 40, 41, 42 and 43 are provided on a semiconductor level, while wiring traces 30, 31, 32 and 33 are provided on a wiring level. Output ports 10, 11, 12 and 13 are each electrically connected to input ports 14, 15, 16 and 17, respectively, via an alignment link. This alignment link is made up of a wiring trace and a buffer block. More particularly, output ports 10, 11, 12 and 13 are connected via wiring traces 30, 31,32 and 33, respectively and buffering blocks 40, 41, 42 and 43 respectively. In short, each alignment link is composed of a wiring trace and a buffering block, all of which are located within the common area 35. Common area 35 is preferably arranged so as to allow for placement of both wiring traces and buffering blocks (circuitry) within the common area, one on top of the other.

Buffering blocks 40, 41, 42 and 43 are designed to maintain the signal quality of the signal as it passes from the output ports 10, 11, 12 and 13 to the input ports 14, 15, 16 and 17 respectively. More particularly, signal timing accuracy is maintained by virtue of the signal buffering blocks 40, 41, 42 and 43. This is most important where output ports 10,11,12 and 13 are a substantial distance from ports 14, 15, 16 and 17 in relation to the overall circuit areas. A substantial distance in this context would typically be any

distance which would negatively impact signal quality as it travels from one set of ports to the another and would typically be viewed by one skilled in the art as requiring buffering to avoid signal degradation.

Fig. 4 illustrates integrated circuit real estate. Here there are shown multiple levels of real estate. There is provided semiconductor level 52 on which semiconductor features are located. There is also provided a wiring level 1 (51) and a wiring level 2 (50) . Wiring traces are located on the wiring levels.

It should be emphasized that the above-described embodiments of the present invention, particularly, any "preferred" embodiments, are merely possible examples of implementations, merely set forth for a clear understanding of the principles of the invention. Many variations and modifications may be made to the above-described embodiment(s) of the invention without departing substantially from the spirit and principles of the invention. All such modifications and variations are intended to be included herein within the scope of the present invention and protected by the following claims.

CLAIMS:

What is claimed:

1. An integrated circuit comprising:

a first port for outputting a signal;

a second port for receiving said signal;

an alignment link for electrically connecting said first port with said second port; and

said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port.

2. An integrated circuit according to claim 1 wherein said alignment link further comprise a wiring trace.

3. An integrated circuit according to claim 1 wherein said alignment link comprises a common area of integrated circuit real estate.

4. An integrated circuit according to claim 1 wherein said first port is located in a first area of integrated circuit real estate.

5. An integrated circuit according to claim 1 wherein said second port is located in a second area of integrated circuit real estate.

6. An integrated circuit according to claim 1 wherein said integrated circuit real estate comprises multi-levels.

7. An integrated circuit according to claim 6 wherein said multi-levels comprise a semiconductor level and a wire tracing level.

8. An integrated circuit according to claim 7 wherein said semiconductor level comprises said signal buffer.

9. An integrated circuit according to claim 7 wherein said wire-tracing level comprises said first port and said second port.

10. An integrated circuit according to claim 9 wherein said wire-tracing level comprises a plurality of levels.

11. A method of aligning ports in an integrated circuit comprising the steps of:

extending a first port from one area into a common area;

extending a second port from a second area into said common area; and

linking said first port to said second port within said common area via an alignment link wherein said alignment link comprises a wiring trace and a signal buffer.

12. A method of aligning ports in an integrated circuit according to claim 11 wherein said common area comprises a multi level area.

13. A method of aligning ports in an integrated circuit according to claim 12 wherein said multi-level area comprises a wiring level and a semiconductor level.

14. A method of aligning ports in an integrated circuit according to claim 13 wherein said semiconductor level comprises said signal buffer.

15. A method of aligning ports in an integrated circuit according to claim 13 wherein said wiring level comprises said wiring trace.

16. A method of aligning ports in an integrated circuit according to claim 11 wherein said first area and said second area are at a substantial distance from each other relative to overall integrated circuit real estate.

17. An integrated circuit comprising :

a first port for outputting a signal;

a second port for receiving said signal; and

an alignment means for electrically connecting said first port with said second port.

18. An integrated circuit according to claim 17 wherein said alignment means comprises a wiring trace and signal buffering circuitry.

19. An integrated circuit according to claim 18 wherein said wiring trace and said signal buffering circuitry occupy a common area of integrated circuit real estate.

20. An integrated circuit according to claim 19 wherein said first port and said second port are located at a substantial distance to each other relative to overall integrated circuit real estate.

ABSTRACT OF THE DISCLOSURE

The present invention relates to a method of integrated circuit construction in which misaligned ports are linked via an alignment link made up of a wiring trace and signal buffer. The signal buffer and wiring trace are located within a common area of integrated circuit real estate.

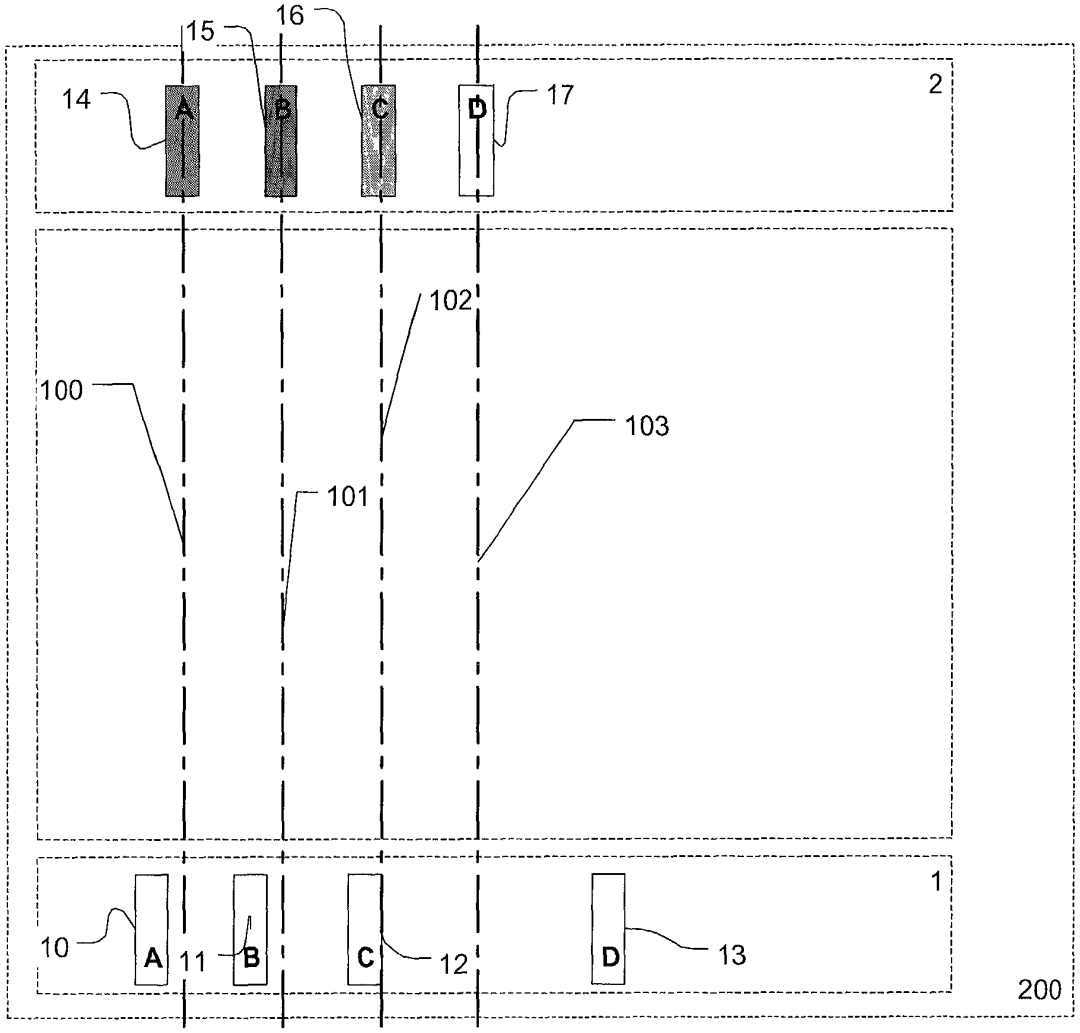

FIG.1

PRIOR ART

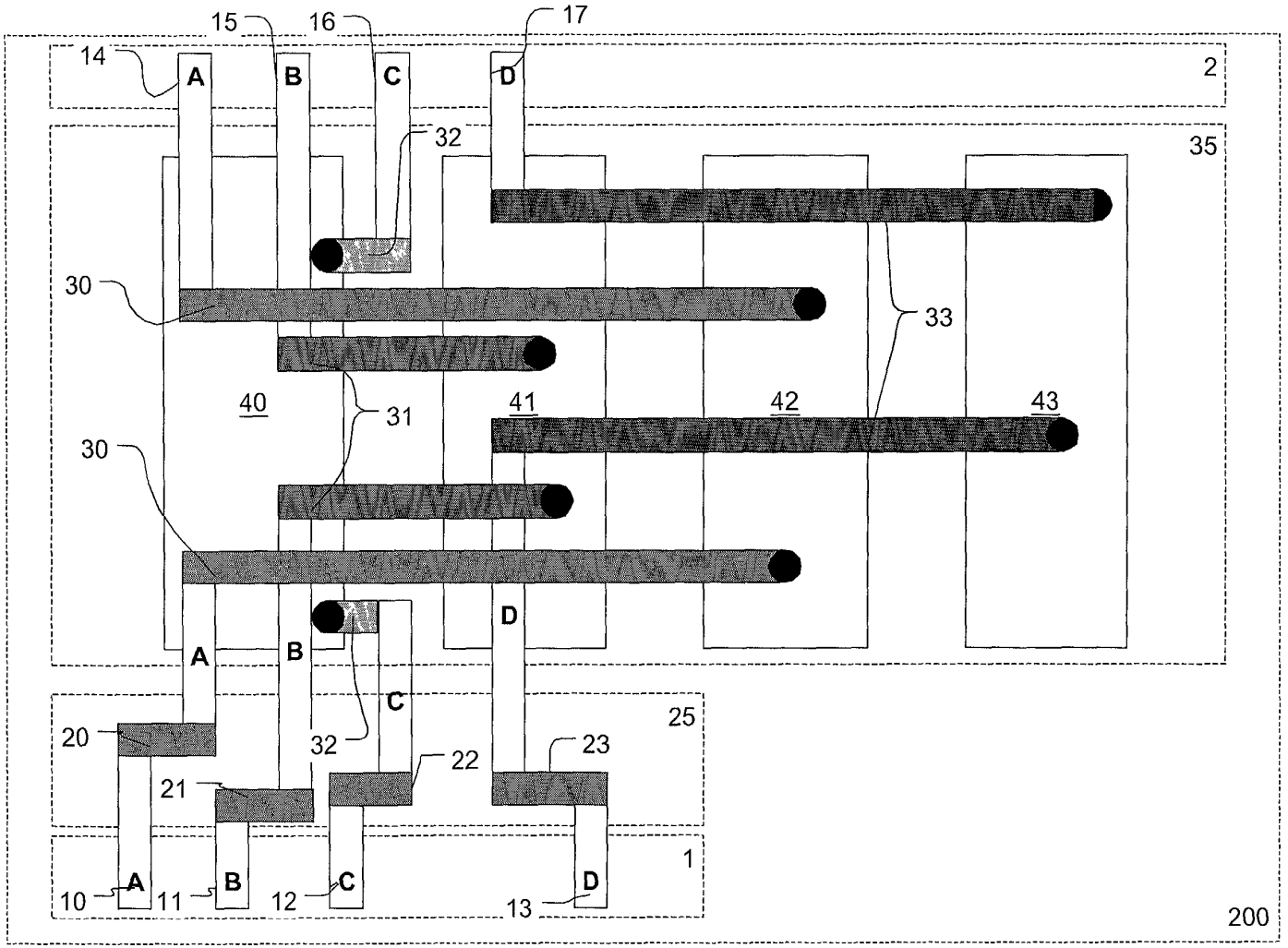

FIG. 2
PRIOR ART

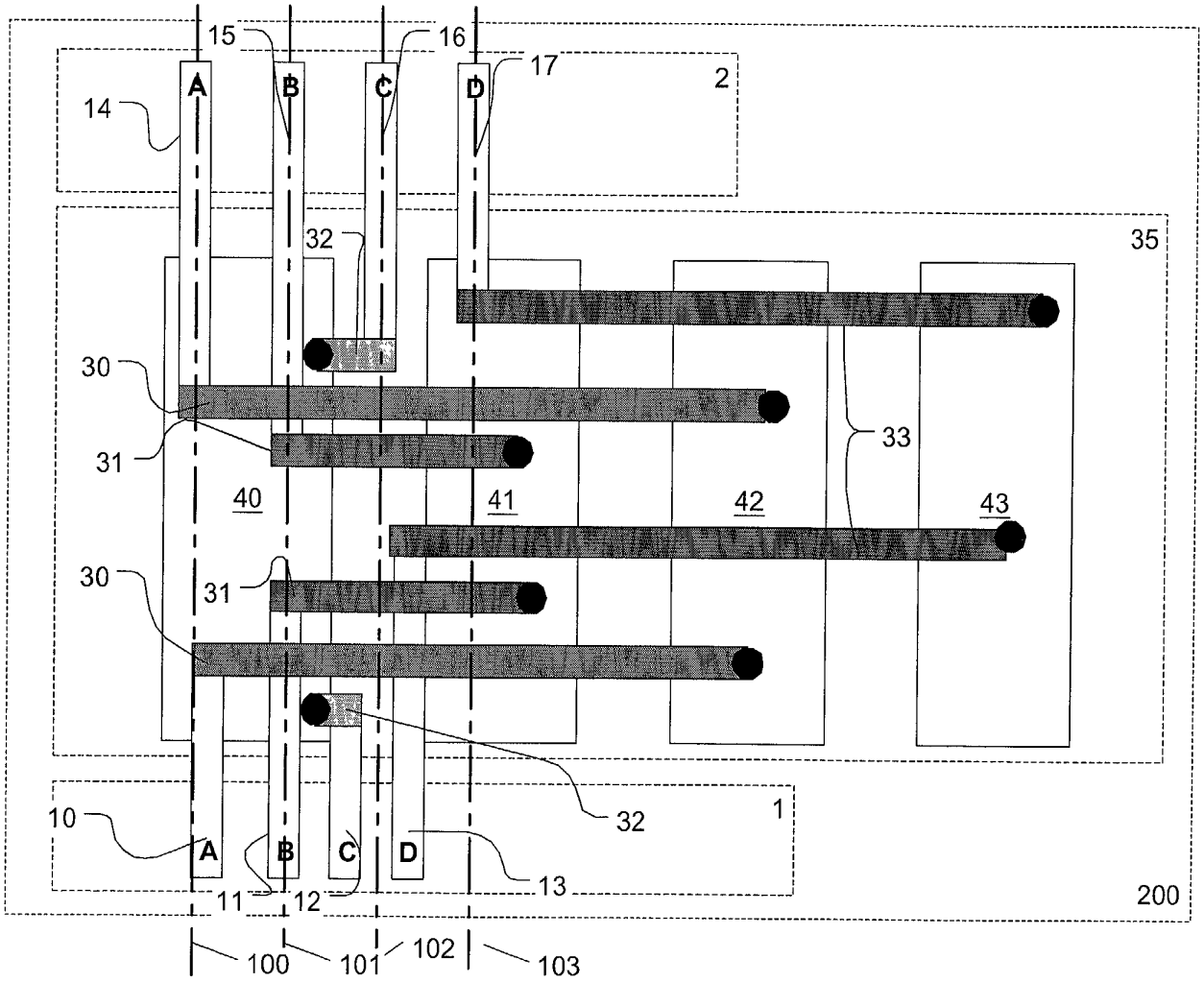
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FIG. 3

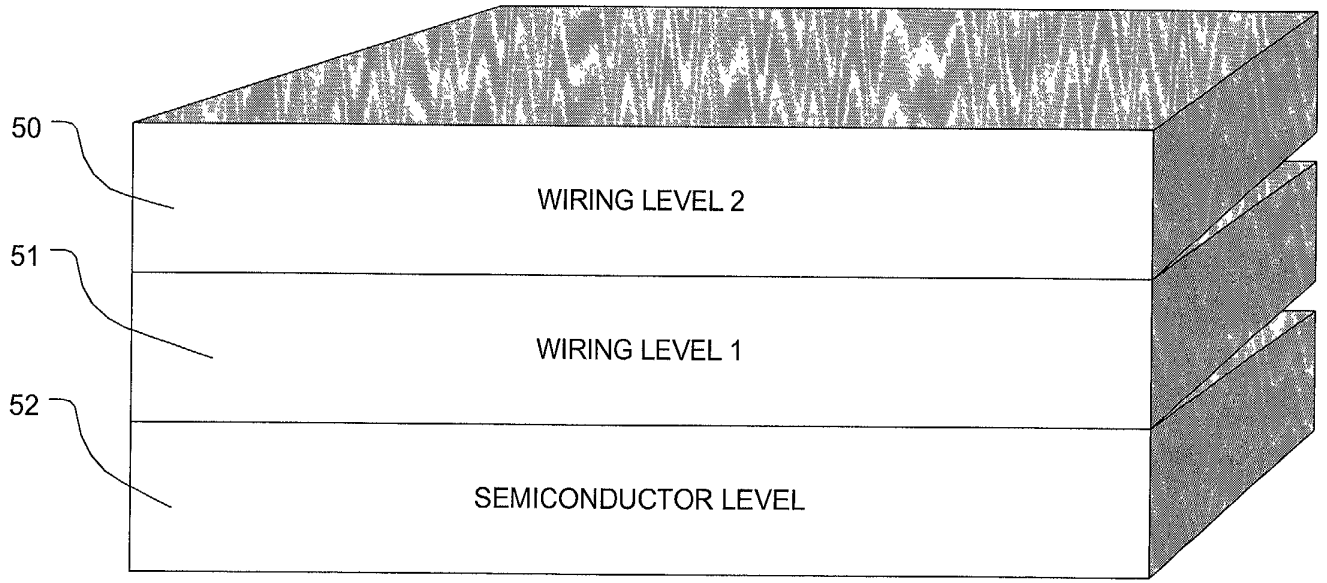

FIG. 4

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 10991989-1

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

A Method Of Integrated Circuit Construction With Port Alignment And Timing Signal Buffering Within A Common Area

the specification of which is attached hereto unless the following box is checked:

( ) was filed on _____ as US Application Serial No. or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: ___ NO: ___
			YES: ___ NO: ___

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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Santa Clara, California 95052-8043

Direct Telephone Calls To:
Cynthia S Mitchell
(970) 679-3136

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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M. Jason Welch
Inventor's Signature

1/20/00
Date

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (continued)

ATTORNEY DOCKET NO. 10991989-1

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Residence: 1107 Twinberry Court Ft Collins CO 80525

Post Office Address: Same as residence

Paul D Nuber 1/20/2000

Inventor's Signature Date

Full Name of # 3 joint inventor: _____ Citizenship: _____

Residence: _____

Post Office Address: _____

Inventor's Signature Date

Full Name of # 4 joint inventor: _____ Citizenship: _____

Residence: _____

Post Office Address: _____

Inventor's Signature Date

Full Name of # 5 joint inventor: _____ Citizenship: _____

Residence: _____

Post Office Address: _____

Inventor's Signature Date

Full Name of # 6 joint inventor: _____ Citizenship: _____

Residence: _____

Post Office Address: _____

Inventor's Signature Date

Full Name of # 7 joint inventor: _____ Citizenship: _____

Residence: _____

Post Office Address: _____

Inventor's Signature Date

Full Name of # 8 joint inventor: _____ Citizenship: _____

Residence: _____

Post Office Address: _____

Inventor's Signature Date